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September 6, 2000

Assistant Commissioner for Patents
Washington, D.C. 20231

Re: New U.S. Patent Application Entitled
BROADBAND SINGLE-ENDED INPUT
UPCONVERTER
Inventors: Yung-Hui Chen, Ting-Yuan Cheng,
and Keng-Li Su
Attorney Docket No.: 06720.0061

Sir:

We enclose the following papers for filing in the U.S. Patent and Trademark Office in connection with the above-identified patent application. Please accord this application a serial number and filing date.

XX Application consisting of 24 pages, including 8 independent claims and 36 claims total.

XX Drawings consisting of 14 sheets of informal drawings.

XX Executed Declaration and Power of Attorney.

_ An executed Declaration and Power of Attorney will be filed after the issuance of a Notice to File Missing Parts, along with the necessary filing and late fees.

XX Executed Assignment to Industrial Technology Research Institute and Recordation Form Cover Sheet. Please record and return the Assignment to the undersigned.

XX A check in the amount of $1408.00 is enclosed (representing a filing fee of $690.00, additional claims fee of $678.00, and assignment fee of $40.00).

_ Claim for Priority in which Applicants claim the right to priority based on ________ Patent Application No. ________ filed ________.

XX Information Disclosure Statement.

XX Please address all correspondence to FINNEGAN, HENDERSON, FARABOW, GARRETT and DUNNER, L.L.P., 1300 I Street, N.W., Washington, D.C. 20005-3315.

The Commissioner is hereby authorized to charge any additional filing fees due and any other fees due under 37 C.F.R. §§ 1.16 or 1.17 during the pendency of this application to Deposit Account No. 06-0916.

Respectfully submitted.

FINNEGAN, HENDERSON, FARABOW,
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ATTORNEY DOCKET NO.: 6720.0061-00

United States Patent Application

of

Yung-Hue CHEN
Ting-Yuan CHENG, and
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for

BROADBAND SINGLE-ENDED INPUT UPCONVERTER

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention pertains in general to a frequency conversion device, and more particularly, a single-ended upconverter.

Description of the Related Art

U.S. Patent No. 5,625,307, to Scheinberg entitled, "Low Cost Monolithic GaAs Upconverter Chip" ("*Scheinberg*") describes an improvement upon a known frequency upconverter employing a Gilbert type double-balanced mixer. *Scheinberg* is hereby incorporated by reference.

A frequency upconverter generally includes an RF amplifier to amplify a radio frequency ("RF") input signal, a local oscillator ("LO") to generate a LO signal, and a mixer to combine the RF input and LO signals to generate an intermediate frequency ("IF") signal. FIG. 1 is a general block diagram of a known upconverter for double-conversion 102. Referring to FIG. 1, upconverter 102 includes a low-noise amplifier ("LNA") 104, a Gilbert type image-rejecting mixer 106, a phase splitter 110, a voltage-controlled oscillator ("VCO") 112 and a DC bias circuit 108. Upconverter 102 also includes sixteen pins, #1 to #16. Pin #6 receives an input signal RF and couples input signal RF to LNA 104, which, in turn, provides a differential output signal to mixer 106 to generate differential IF signals at ports #1 and #16. Differential IF signals have frequencies higher than that of the input RF signal.

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FIG. 2 is a functional block diagram of LNA 104 and mixer 106 of FIG. 1. Referring to FIG. 2, input signal RF is transformed into a differential pair, RF^+ and RF^-, through an external capacitor-inductor-capacitor circuit 114. Differential pair RF^+ and RF^- may also be created through an alternative embodiment of a Balun circuit 114A. LNA 104 receives differential pair RF^+ and RF^- as input signals and provide output signals to mixer 106. Mixer 106 additionally receives differential signals LO to generate differential IF signals. Because LNA 104 requires differential-pair RF input signals, an external circuit, one such as Balun circuit 114, is always required. Such an external circuit is disadvantageous because it occupies additional chip area on a semiconductor wafer. FIG. 3 shows a schematic diagram of FIG. 2 as described in *Scheinberg*.

FIG. 4 is a functional block diagram of a conventional differential-pair input upconverter employing RF bypass networks. Referring to FIG. 4, an RF bypass network 116 is disposed between the input terminals of LNA 104 and differential-pair signals RF^+ and RF^-. RF bypass network 116 includes a first resistor 118, a second resistor 120, and a capacitor 122 connected in series. One end of capacitor 122 is coupled to resistor 120 and the other end of capacitor 122 is coupled to ground. RF bypass network 116 functions to dampen potential resonances of upconverter 102 created by bond wires (not shown) or the parasitic self-inductances of the package pins (not shown). However, RF bypass network 116 lacks preferred resistance matching at the input end of upconverter 102 and control of high-frequency image signals. FIG. 5 is a schematic diagram of FIG. 4.

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FIG. 6 is a schematic diagram of a conventional differential-pair input upconverter including source degeneration networks. Referring to FIG. 6, LNA of upconverter 102 includes a first transistor 138, a second transistor 140, and a source degeneration network 124. Source degeneration network 124 includes matched source-degenerating inductors 126 and 128 and resistors 142 and 144 to eliminate noise created by transistors 138 and 140 and control image noise. Another embodiment of a source degeneration network is shown as 124A, including only source degenerating inductors. Although source degeneration resistors 142 and 144 improve the linearity of transistors 138 and 140 of LNA 104, source degeneration resistors 142 and 144 also decrease the gain of LNA 104. Similarly, although source degeneration inductors 126 and 128 inhibit image noise, inductors 126 and 128 do not provide for the linearity, conversion gain, or noise figure characteristics of LNA 104 or mixer 106.

Scheinberg additionally describes a DC bias circuit to address long power-up latencies in the order of several seconds, which cause an increased testing time. FIG. 7 is a schematic diagram of *Scheinberg* including a DC bias circuit that includes resistors 130, 132, and 134. A passive voltage-dividing network is shown in FIG. 7. The gate of transistor 136, which functions as a current source, is biased by the voltage-dividing network comprising resistor 130, 132, and 134, which act to prevent power-up latency. However, this design complicates the overall circuit design of upconverter 102.

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Furthermore, when a upconverter chip is packaged, an external resonator is coupled to an internal VCO. The external resonator is grounded directly to an internal ground node of the upconverter chip or a ground node of the Printed Circuit Board (PCB). As a result, noise generated by the external resonator may be coupled to the internal VCO or other internal components of the upconverter through the common ground connection.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to an improved upconverter that substantially obviates one or more problems due to limitations and disadvantages of the prior art.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structures and methods particularly pointed out in the written description and claims thereof, as well as the appended drawings.

To achieve these and other advantages, and in accordance with the purpose of the invention as embodied and broadly described, there is provided an upconverter for modulating an input signal to provide an output signal having a higher frequency, which includes a mixer and an amplifier, coupled to the mixer, including a plurality of transistors and having a first input terminal for receiving the input signal and a

second input terminal for receiving a DC power control signal of a predetermined level, wherein the DC power control signal turns off the transistors of the amplifier when the predetermined level is between approximately -1 to -2 volts.

In one aspect of the invention, the upconverter further includes a source degenerating inductor circuit including a first inductor in parallel with a second inductor and a third inductor thereby forming a "Y"-shaped circuit, wherein the first inductor has a higher inductance than the second and third inductors.

In another aspect of the invention, the upconverter further includes a DC bias network for biasing the mixer and reducing power-up latency in the upconverter including a voltage dividing network coupled to the second input terminal of the amplifier.

In yet another aspect of the invention, wherein the DC bias network comprises first, second, third, and fourth resistors, the first resistor and third resistor receive a differential LO signal and the first resistor is in parallel with the second resistor, the third resistor, and the fourth resistor.

In still another aspect of the invention, the upconverter additionally includes a plurality of serially connected diodes coupled to the first input terminal of the amplifier for electro-static discharge protection.

Also in accordance with the present invention, there is provided an upconverter for modulating an input signal to provide an output signal having a higher frequency that includes a mixer and an amplifier, coupled to the mixer, including matched first and second MESFETs, each MESFET having source, gate,

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and drain terminals, wherein the gate of the first MESFET receives the input signal, and the gate of the second MESFET is coupled to a DC control voltage capable of turning off the first and second MESFETs.

Additionally in accordance with the present invention, there is provided an upconverter for modulating an input signal to provide an output signal having a higher frequency, the input signal including an image signal, which upconverter includes a mixer, an amplifier, coupled to the mixer circuit, including a first input terminal for receiving the input signal, a second input terminal coupled to ground, and a filter for rejecting noise signals having a same frequency as the image signal of the input signal, and a first resistor having a first end coupled to the first input terminal of the amplifier and a second end coupled to ground.

In one aspect of the invention, the amplifier comprises matched first and second MESFETs, each MESFET having source, gate, and drain terminals, wherein the gate of the first MESFET receives an input signal and is coupled to one end of a filter, and the gate of the second MESFET is coupled to ground and a second end of the filter.

In another aspect of the invention, the mixer comprises matched third and fourth MESFETs, each having source, gate and drain terminals, and matched fifth and sixth MESFETs, each having source, gate and drain terminals, wherein the sources of the third and fourth MESFETs are coupled to the drain of the first MESFET and the sources of the fifth and sixth MESFETs are coupled to the drain of the second MESFET, the gate of the third MESFET is coupled to the gate of the sixth MESFET and the gate of the fourth MESFET is coupled to the gate of the fifth MESFET, the

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gates of the third and fourth MESFETs receive a differential LO signal, the drain of the third MESFET is coupled to the drain of the fifth MESFET and the drain of the fourth MESFET is coupled to the drain of the sixth MESFET, and the drains of the third and fourth MESFETs provide an IF output signal.

Further in accordance with the present invention, there is provided an upconverter for modulating an input signal to provide an output signal having a higher frequency, which includes a mixer, an amplifier coupled to the mixer, having a first input terminal for receiving the input signal and a second input terminal for receiving a DC power control signal, and a DC bias network for biasing the mixer and reducing power-up latency in the upconverter including a voltage dividing network coupled to the second input terminal of the amplifier and a resistive network coupled to the amplifier.

Also in accordance with the present invention, there is provided an upconverter for mixing a single-ended RF signal with a differential LO signal to generate a differential IF signal that includes a source degenerated first differential pair comprising matched first and second transistors, each having source, gate and drain terminals, wherein the gate of the first transistor receives an input signal and the gate of the second transistor is connected to a ground potential, and a second differential pair comprising matched third and fourth transistors, each having source, gate and drain terminals, and a third differential pair comprising matched fifth and sixth transistors, each having source, gate and drain terminals, wherein the sources of the third and fourth transistors are coupled to the drain of the first transistor and the sources of the fifth and sixth transistors are coupled to the drain of the second

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transistor, the gate of the third transistor is coupled to the gate of the fifth transistor and the gate of the fourth transistor is coupled to the gate of the sixth transistor, the drain of the third transistor is coupled to the drain of the sixth transistor and the drain of the fourth transistor is coupled to the drain of the fifth transistor, the gates of the third and fourth transistors receive the differential LO signal, the drains of the third and fourth transistors supply the differential IF signal, the gate of the first transistor is coupled to the single-ended RF signal, and the gate of the second transistor is coupled to a DC control signal.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the objects, advantages, and principles of the invention.

In the drawings:

FIG. 1 is a block diagram of a conventional upconverter;

FIG. 2 is a functional block diagram of a conventional differential-pair input upconverter;

FIG. 3 is a schematic diagram of FIG. 2;

FIG. 4 is a functional block diagram of a conventional differential-pair input upconverter including a RF bypass network;

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FIG. 5 is a schematic diagram of FIG. 6;

FIG. 6 is a schematic diagram of a conventional differential-pair input upconverter including source degeneration networks;

FIG. 7 is a schematic diagram of a conventional differential-pair input upconverter including a DC bias circuit;

FIG. 8 is a functional block diagram of one embodiment of the present invention;

FIG. 9 is a schematic diagram of FIG. 8;

FIG. 10 is a schematic diagram of another embodiment of the present invention including an image rejection filter and a matching resistor;

FIG. 11 is a schematic diagram of one embodiment of the present invention that includes a source degenerating circuit;

FIG. 12 is a schematic diagram of one embodiment of the present invention that includes a DC bias circuit;

FIG. 13 is a schematic diagram of one embodiment of the present invention that includes an electrostatic discharge protection circuit; and

FIG. 14 is a block diagram of a packaged upconverter chip according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 8 is a functional block diagram of one embodiment of the present invention. Referring to Fig. 8, an upconverter 2 includes a low noise amplifier ("LNA") 4 coupled to a Gilbert-type mixer 6. LNA 4 includes a first input terminal 8

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and a second input terminal 10. First input terminal 8 receives a single-ended input RF signal and second input terminal 10 receives a DC power control signal of a predetermined level. A single-ended RF input obviates the need for an external balun circuit to create differential pair RF signals. A single-ended upconverter is advantageous over a differential-pair upconverter in cost and simplicity of circuit design.

Mixer 6 receives input signals from LNA 4 and differential signals from LO to generate differential-pair output signals IF. In one embodiment of the invention, the DC power control signal turns off LNA 4 when the predetermined level is, for example, between approximately -1 to -2 volts. LNA 4 may be optionally turned off by the DC power control signal such that mixer 6 will not generate any differential-pair output signals thereby achieving output power control. When upconverter 2 is in operation, the DC power control signal is turned off.

FIG. 9 is a schematic diagram of FIG. 8. Referring to FIG. 9, LNA 4 includes transistors 42 and 44 and a mixer 6 including transistors 62, 64, 66 and 68. Each of transistors 42, 44, 62, 64, 66 and 68 may be a metal semiconductor field effect transistor ("MESFET"). In one embodiment of the present invention, transistors 42 and 44, transistors 62 and 64, and transistors 66 and 68, are each matched transistor pairs. The gate of transistor 42 is provided as first input terminal 8 of LNA 4, and the gate of transistor 44 is provided as second input terminal 10 of LNA 4. The drain of transistor 42 is coupled to the source of transistor 62 and the source of transistor 64. The drain of transistor 44 is coupled to the source of transistor 66 and transistor 68. The gates of transistors 62 and 68 receive a differential LO^- signal, and the gates of

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transistor 64 and 66 receive a differential LO^+ signal. The drain of transistor 62 is coupled to the drain of transistor 66 to provide differential output signal IF^+. The drain of transistor 68 is coupled to the drain of 64 to provide differential output signal IF^-.

First input terminal 8 and second input terminal 10 are each coupled to a bond wire 12. First input terminal 8 receives a single-ended RF input signal through bond wire 12. Second input terminal 10 receives a DC power control signal through bond wire 12. In one embodiment of the present invention, the DC power control signal turns off transistors 42 and 44 when the predetermined DC power control signal level is between, for example, approximately -1 to -2 volts.

FIG. 10 is a schematic diagram of another embodiment of the present invention in which LNA 4 includes transistor 42, transistor 44, and an image rejection filter 14 to reject noise signals having the same frequency as the image signal of the input RF signal. Referring to FIG. 10, image rejection filter 14 is coupled at one end to the gate of transistor 42 and coupled at the other end to the gate of transistor 44. In one embodiment, image rejection filter 14 is a low-pass filter and includes a capacitor 140 connected in series with an inductor 142, and the capacitor-inductor pair is parallel with resistor 144. In operation, image rejection filter 14 filters out image harmonics to improve image rejection and acts as a noise filter.

FIG. 10 further includes a matching resistor 16 coupled at one end to the gate of transistor 42 through bond wired 12 and coupled to ground at the other end to reject potential resonances of upconverter 2 created by bond wires or parasitic self-inductances of the package pins at first input terminal 8. Resistor 16 matches the

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input impedance with that of the upconverter, and the value of which depends on upconverter characteristics. The matching resistor may be implemented as a matching impedance to improve performance. The image rejection filter and matching resistor provide an improved resistance matching and image signal control.

FIG. 11 is a schematic diagram of one embodiment of the present invention that includes a source degenerating circuit 18 coupled to LNA 4. Source degenerating circuit 18 is coupled at one end to the source of transistor 42 and at the other end to the source of transistor 44 of LNA 4. Source degenerating circuit 18 includes a first inductor 180 coupled in parallel with a second inductor 182 and a third inductor 184, thereby forming a "Y"-shaped circuit. First inductor 180 is coupled to ground through bond wire 12. In one embodiment of the present invention, a resistor 20 is disposed between bond wire 12 and ground. In another embodiment of the present invention, first inductor 180 has a higher inductance than second inductor 182 and third inductor 184. In one embodiment of the invention, inductor 180 has a value six times as great as that of inductor 182. Similarly, inductor 180 has a value six time as great as that of inductor 184.

In operation, second inductor 182 and third inductor 184 together act as a high-pass filter to substantially eliminate high frequency image noise. First inductor 180 is a low-pass filter that substantially eliminates input noises coupled through from the ground connection. Source degeneration circuit 18 of the present invention eliminates noise to improve linearity of LNA 4 and mixer 6, and at the same time, preserves the gain and noise figure characteristics of LNA 4.

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FIG. 12 is a schematic diagram of one embodiment of the present invention that includes a DC bias circuit. Referring to FIG. 12, there includes an internal DC bias circuit 22 and an external DC bias circuit 24. Internal DC bias circuit 22 is coupled at one end to a voltage source V_{dc}. DC bias circuit 22 is coupled at the other end to the gate of transistor 44 of LNA 4 and the DC power control signal through bond wire 12. DC bias circuit 22 comprises a voltage dividing network including a plurality of resistors 26, 28, 30, and 32, to provide the voltages requires by LNA 4 and mixer 6. Resistor 32 is in parallel with resistors 30, 26 and 28. Resistor 32 receives differential LO^+ signal and resistor 30 receives differential LO^- signal. Resistor 26 receives a DC voltage through bond wire 12, and resistor 28 is coupled at one end to the gate of transistor 44 and the DC power control signal through bond wire 12. External DC bias circuit 24 adjusts the conversion gain, linearity and DC current of LNA 4. This embodiment of the present invention provides a simplified circuit to prevent power-up latency.

FIG. 13 is a schematic diagram of one embodiment of the present invention that includes an electro-static discharge ("ESD") protection circuit 34. Referring to FIG. 13, ESD protection circuit includes a plurality of diode-connected transistors. In one embodiment, as shown in FIG. 13, four diode-connected transistors are able to withstand an ESD discharge of more than -2kV. In one embodiment of the invention, each of diode-connected transistor has a bias voltage of 0.7 volts.

FIG. 14 is a block diagram of a packaged upconverter chip of the present invention. Referring to FIG. 14, an upconverter chip (not numbered) include packaging 40, a leadframe 38 disposed over packaging 40, a semiconductor die

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containing an upconverter 2 disposed over leadframe 38, and a plurality of packaging pins. An external resonator circuit 36 is coupled to a GND pin and V_{DDLO} pin of the upconverter chip, which includes a plurality of ground (GND) pins. Each of the plurality of GND pins is coupled to leadframe 38 through bond wires 12. Leadframe 38 absorbs noises generated by external resonator circuit 36 to prevent the noise from being coupled to any components of upconverter.

It will be apparent to those skilled in the art that various modifications and variations can be made in the disclosed product without departing from the scope or spirit of the invention. Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

WHAT IS CLAIMED IS:

1. An upconverter for modulating an input signal to provide an output signal having a higher frequency than said input signal than the input signal, comprising:

a mixer; and

an amplifier coupled to the mixer, including a plurality of transistors and having a first input terminal for receiving the input signal and a second input terminal for receiving a DC power control signal of a predetermined level, wherein the DC power control signal turns off the transistors of the amplifier when the predetermined level is between approximately -1 to -2 volts.

2. The upconverter as claimed in claim 1 further comprising a source degenerating inductor circuit including a first inductor in parallel with a second inductor and a third inductor, wherein the first inductor has a higher inductance than each of the second inductor and the third inductor.

3. The upconverter as claimed in claim 1 further comprising a DC bias network for biasing the mixer and reducing power-up latency in the upconverter including a voltage dividing network coupled to the second input terminal of the amplifier.

4. The upconverter as claimed in claim 3, wherein the DC bias network comprises a first resistor, a second resistor, a third resistor, and a fourth resistor, the first resistor and third resistor receiving a differential local oscillator signal and the first resistor being in parallel with each of the second resistor, the third resistor, and the fourth resistor.

5. The upconverter as claimed in claim 1 further comprising a plurality of serially connected diodes coupled to the first input terminal of the amplifier for electro-static discharge protection.

6. The upconverter as claimed in claim 5, wherein the plurality of serially connected diodes comprises a plurality of diode-connected transistors.

7. An upconverter for modulating an input signal to provide an output signal having a higher frequency than the input signal, comprising:

a mixer; and

an amplifier, coupled to the mixer, including matched first and second MESFETs, each MESFET having source, gate, and drain terminals, wherein the gate of the first MESFET receives the input signal, and the gate of the second MESFET is coupled to a DC control voltage capable of turning off the first and second MESFETs.

8. The upconverter as claimed in claim 7 further comprising a plurality of diode-connected MESFETs to protect the upconverter from electro-static discharge.

9. The upconverter as claimed in claim 7 further comprising a source degenerating inductor circuit coupled to the amplifier to reduce noise.

10. The upconverter as claimed in claim 9, wherein the source degenerating inductor circuit comprises a first inductor coupled in parallel with a second inductor and a third inductor.

11. The upconverter as claimed in claim 10, wherein the first inductor has a higher inductance than each of the second inductor and the third inductor.

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12. The upconverter as claimed in claim 7 further comprising a DC bias network for biasing the mixer and reducing power-up latency in the upconverter including a voltage dividing network coupled to the second input terminal of the amplifier.

13. An upconverter for modulating an input signal to provide an output signal having a higher frequency, the input signal including an image signal, comprising:

a mixer;

an amplifier, coupled to the mixer circuit, including

a first input terminal for receiving the input signal,

a second input terminal coupled to ground, and

a filter for rejecting noise signals having a same frequency as the image signal of the input signal; and

a first resistor having a first end coupled to the first input terminal of the amplifier and a second end coupled to ground.

14. The upconverter as claimed in claim 13, wherein the filter comprises a second resistor having a same resistance as the first resistor.

15. The upconverter as claimed in claim 13, wherein the filter comprises a resistor in parallel with a serial capacitor and inductor pair.

16. The upconverter as claimed in claim 13, wherein the amplifier comprises matched first and second MESFETs, each MESFET having source, gate, and drain terminals, wherein the gate of the first MESFET receives the input signal and is coupled to one end of the filter, and the gate of the second MESFET is coupled to ground and a second end of the filter.

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17. The upconverter as claimed in claim 16, wherein the mixer comprises matched third and fourth MESFETs, each having source, gate and drain terminals, and matched fifth and sixth MESFETs, each having source, gate and drain terminals,

wherein the sources of the third and fourth MESFETs are coupled to the drain of the first MESFET and the sources of the fifth and sixth MESFETs are coupled to the drain of the second MESFET, the gate of the third MESFET is coupled to the gate of the sixth MESFET and the gate of the fourth MESFET is coupled to the gate of the fifth MESFET, the gates of the third and fourth MESFETs receive a differential local oscillator signal, the drain of the third MESFET is coupled to the drain of the fifth MESFET and the drain of the fourth MESFET is coupled to the drain of the sixth MESFET, and the drains of the third and fourth MESFETs providing an IF output signal.

18. The upconverter as claimed in claim 13 further comprising a DC bias network for biasing the mixer and reducing power-up latency in the upconverter including a voltage dividing network coupled to the second input terminal of the amplifier.

19. The upconverter as claimed in claim 13 further comprising a plurality of diode-connected MESFETs to protect the upconverter from electro-static discharge.

20. An upconverter for modulating an input signal to provide an output signal having a higher frequency than the input signal, comprising:

a mixer;

an amplifier, coupled to the mixer, having a first input terminal for receiving the input signal and a second input terminal for receiving a DC power control signal; and

a source degenerating inductor circuit coupled to the amplifier to reduce image noise.

21. The upconverter as claimed in claim 20, wherein the DC control voltage coupled to the second terminal of the mixer turns off the amplifier when the DC control voltage is at a predetermined voltage level.

22. The upconverter as claimed in claim 21, wherein the predetermined voltage level of the DC power control signal is between approximately -1 to -2 volts.

23. The upconverter as claimed in claim 20, wherein the source degenerating inductor circuit comprises a first inductor in parallel with a second inductor and a third inductor.

24. The upconverter as claimed in claim 23, wherein the first inductor has a higher inductance than each of the second inductor and the third inductor.

25. The upconverter as claimed in claim 20 further comprising a DC bias network for biasing the mixer and reducing power-up latency in the upconverter including a voltage dividing network coupled to the second input terminal of the amplifier.

26. The upconverter as claimed in claim 25, wherein the DC bias network comprises a first resistor, a second resistor, a third resistor, and a fourth resistor, the first resistor and third resistor receiving a differential local oscillator signal and the first resistor being in parallel with the second resistor, the third resistor, and the fourth resistor.

27. The upconverter as claimed in claim 20 further comprising a plurality of serially connected diodes coupled to the first input terminal of the amplifier to protect the upconverter from electro-static discharge.

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28. The upconverter as claimed in claim 27, wherein the plurality of serially connected diodes comprise a plurality of diode-connected MESFETs.

29. An upconverter for modulating an input signal to provide an output signal having a higher frequency, comprising:

a mixer;

an amplifier, coupled to the mixer, having a first input terminal for receiving the input signal and a second input terminal for receiving a DC power control signal; and

a DC bias network for biasing the mixer and reducing power-up latency in the upconverter including a voltage dividing network coupled to the second input terminal of the amplifier and a resistive network coupled to the amplifier.

30. The upconverter as claimed in claim 29, wherein the DC bias network comprises a first resistor, a second resistor, a third resistor, and a fourth resistor, the first resistor and third resistor receiving a differential local oscillator signal and the first resistor being in parallel with the second resistor, the third resistor, and the fourth resistor.

31. An upconverter for modulating an input signal to provide an output signal having a higher frequency, comprising:

a mixer;

an amplifier, coupled to the mixer, having a first input terminal for receiving the input signal and a second input terminal for receiving a DC power control signal; and

a plurality of serially connected diode-connected MESFETs coupled to the first input terminal of the amplifier for prevention of electro-static discharge.

32. An upconverter for mixing a single-ended RF signal with a differential local oscillator signal to generate a differential IF signal, comprising:

a source degenerated first differential pair comprising matched first and second transistors, each having source, gate and drain terminals, wherein the gate of the first transistor receives the input signal and the gate of the second transistor receives a ground potential; and

a second differential pair comprising matched third and fourth transistors, each having source, gate and drain terminals, and a third differential pair comprising matched fifth and sixth transistors, each having source, gate and drain terminals,

wherein the sources of the third and fourth transistors are coupled to the drain of the first transistor and the sources of the fifth and sixth transistors are coupled to the drain of the second transistor, the gate of the third transistor is coupled to the gate of the fifth transistor and the gate of the fourth transistor is coupled to the gate of the sixth transistor, the drain of the third transistor is coupled to the drain of the sixth transistor and the drain of the fourth transistor is coupled to the drain of the fifth transistor, the gates of the third and fourth transistors receive the differential local oscillator signal, the drains of the third and fourth transistors supply the differential IF signal, the gate of the first transistor is coupled to the single-ended RF signal, and the gate of the second transistor is coupled to a DC control signal.

33. The upconverter as claimed in claim 32, wherein the DC control voltage

coupled to the gate of the second transistor turns off the first and second transistors when the DC control voltage is at a predetermined voltage level.

34. The upconverter as claimed in claim 32 further comprising a source degenerating inductor circuit coupled to the sources of the first and second transistors to reduce noise, the source degenerating inductor circuit including a first inductor coupled in parallel with a second inductor and a third inductor.

35. The upconverter as claimed in claim 34, wherein the first inductor has a higher inductance than each of the second inductor and the third inductor.

36. An upconverter chip, comprising:

a semiconductor packaging including a plurality of pins;

a leadframe disposed over the packaging; and

a semiconductor die containing an upconverter disposed over the leadframe, wherein the plurality of pins include a plurality of ground pins, each of the plurality of ground pins coupled to the leadframe to substantially eliminate noise coupled from an external resonator.

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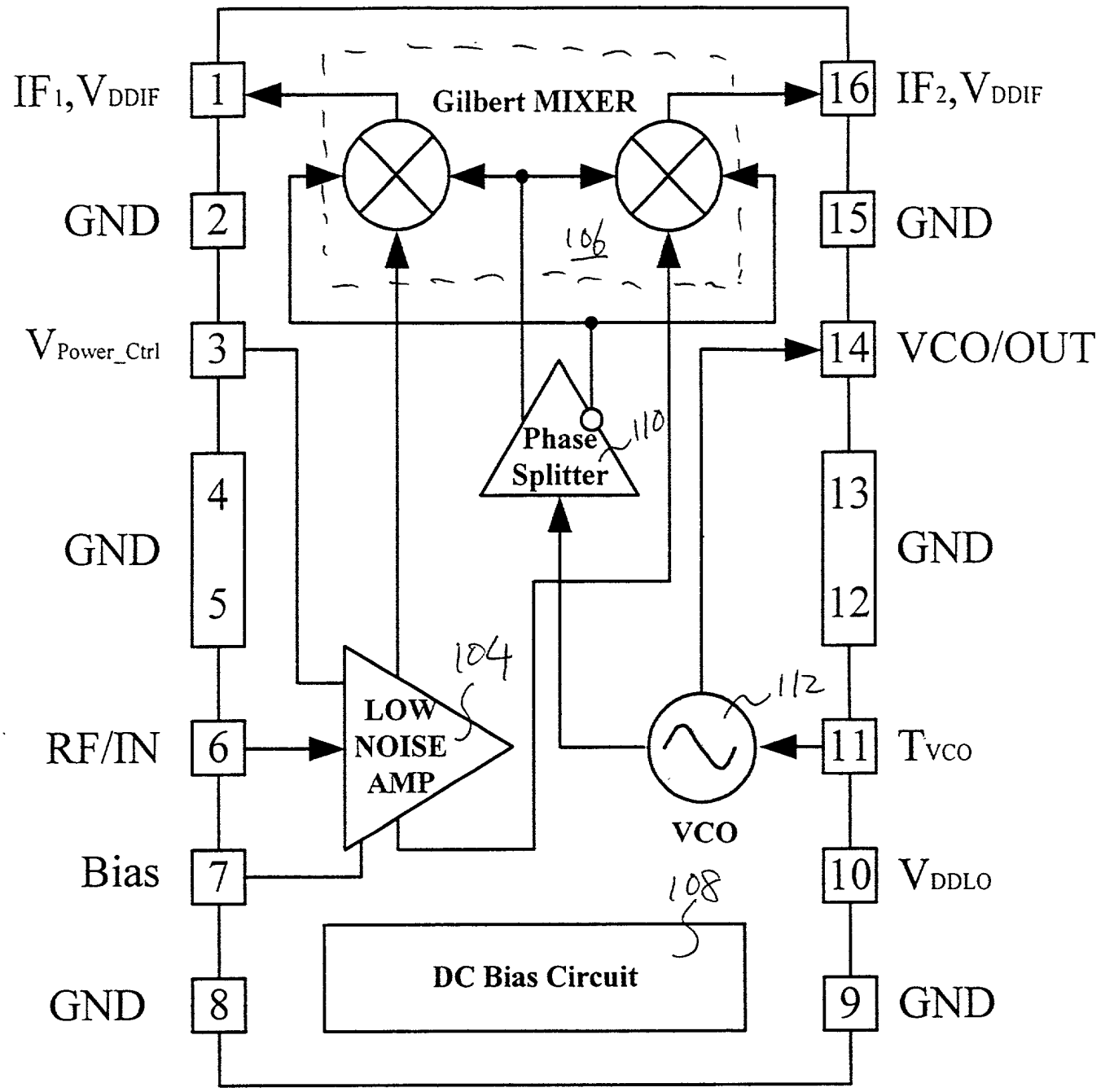
ABSTRACT OF THE DISCLOSURE

An upconverter for mixing a single-ended RF signal with a differential local oscillator signal to generate a differential IF signal, that includes a source degenerated first differential pair comprising matched first and second transistors, each having source, gate and drain terminals, wherein the gate of the first transistor receives the input signal and the gate of the second transistor receives a ground potential, and a second differential pair comprising matched third and fourth transistors, each having source, gate and drain terminals, and a third differential pair comprising matched fifth and sixth transistors, each having source, gate and drain terminals, wherein the sources of the third and fourth transistors are coupled to the drain of the first transistor and the sources of the fifth and sixth transistors are coupled to the drain of the second transistor, the gate of the third transistor is coupled to the gate of the fifth transistor and the gate of the fourth transistor is coupled to the gate of the sixth transistor, the drain of the third transistor is coupled to the drain of the sixth transistor and the drain of the fourth transistor is coupled to the drain of the fifth transistor, the gates of the third and fourth transistors receive the differential local oscillator signal, the drains of the third and fourth transistors supply the differential IF signal, the gate of the first transistor is coupled to the single-ended RF signal, and the gate of the second transistor is coupled to a DC control signal.



102

Fig. 1

PRIOR ART

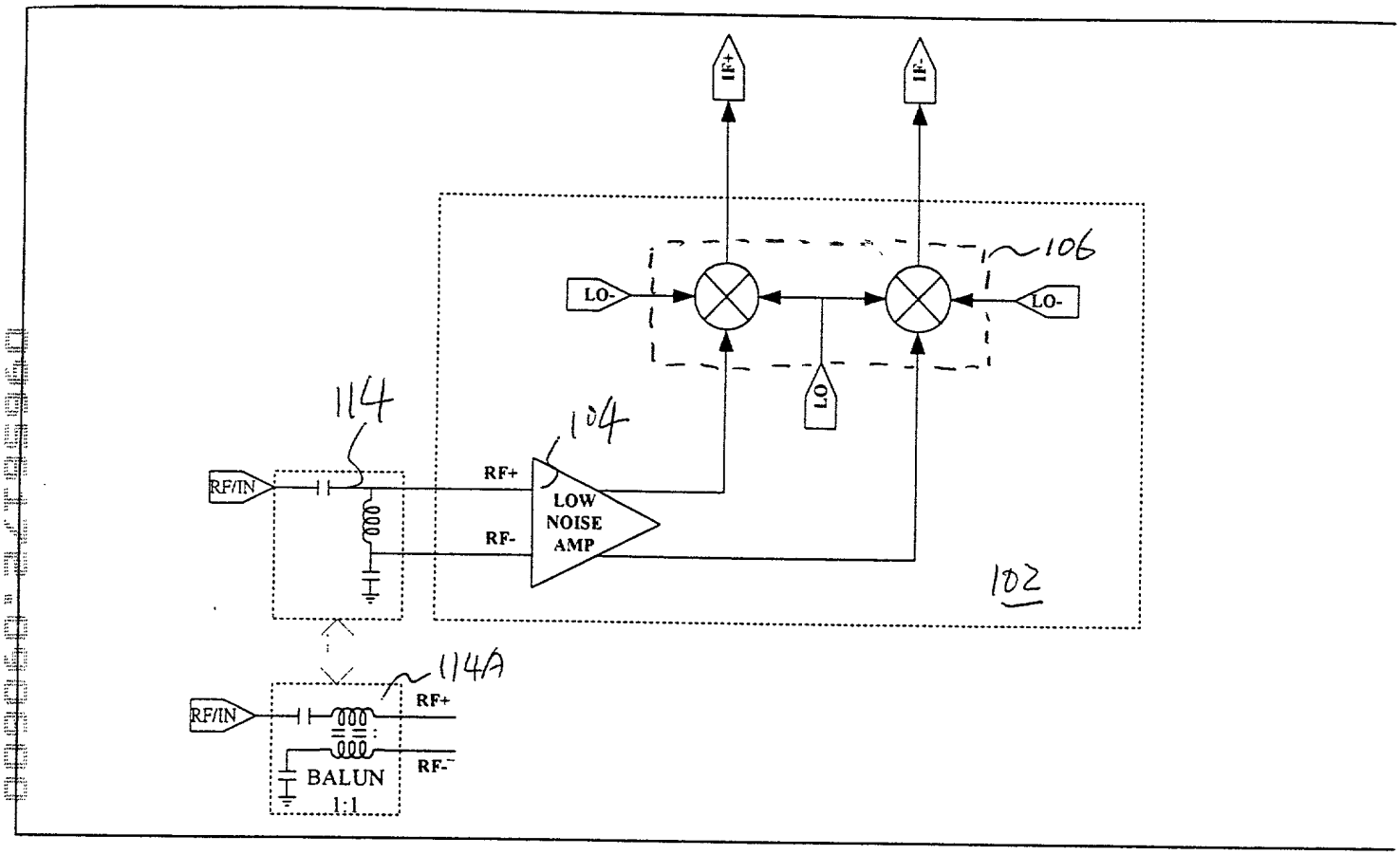


Fig. 2

PRIOR ART

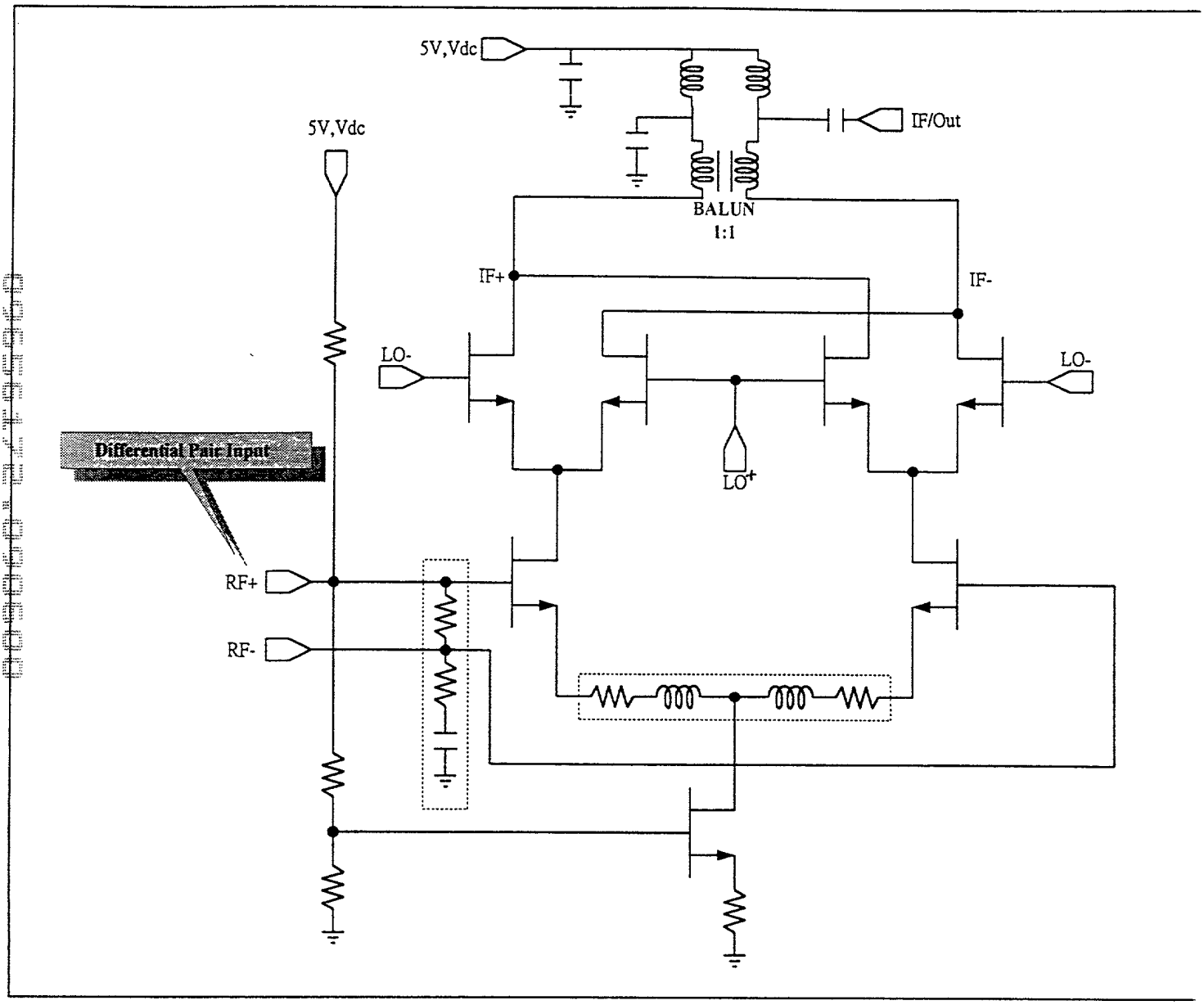


Fig. 3

PRIOR ART

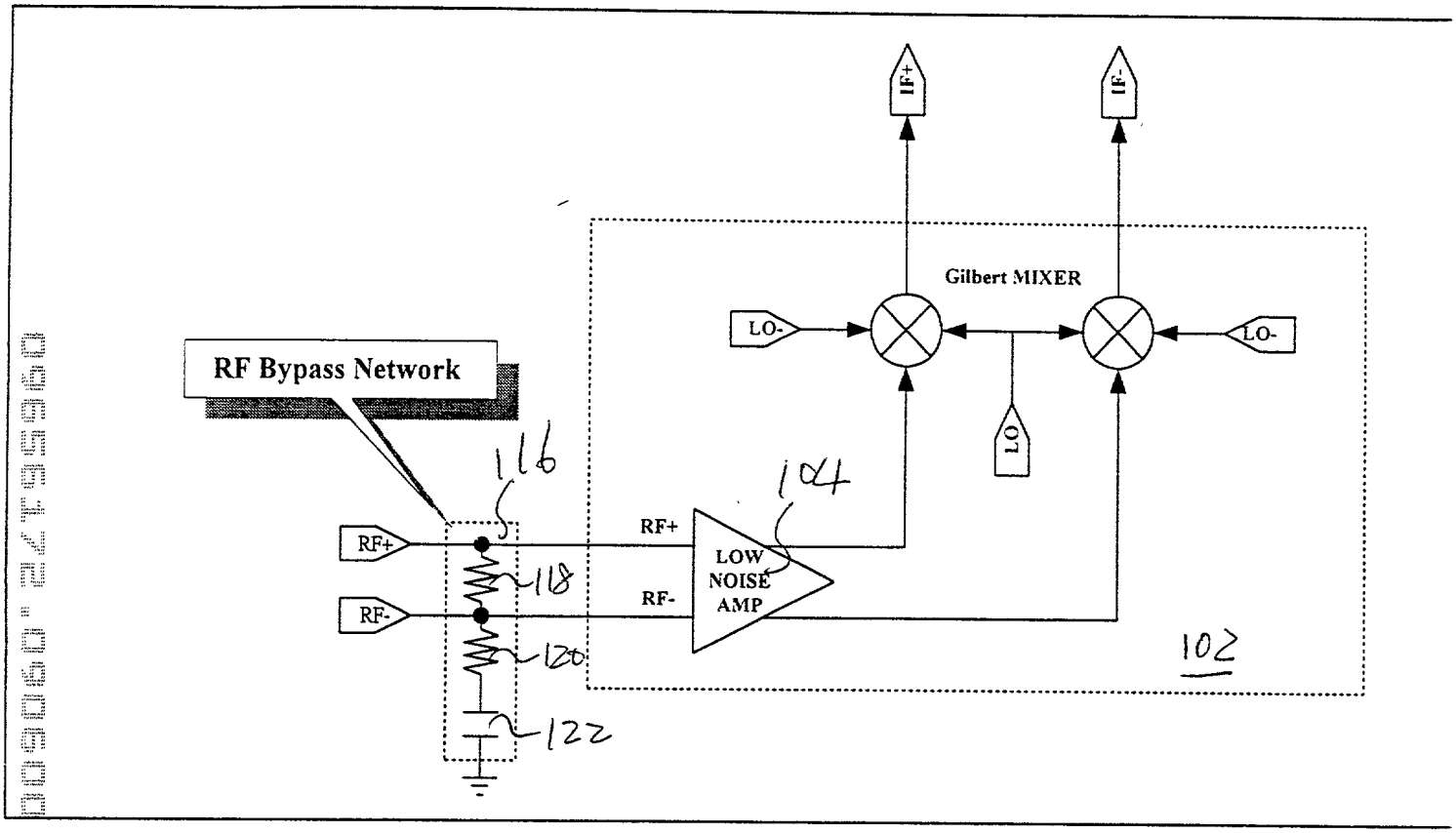


Fig. 4
PRIOR ART

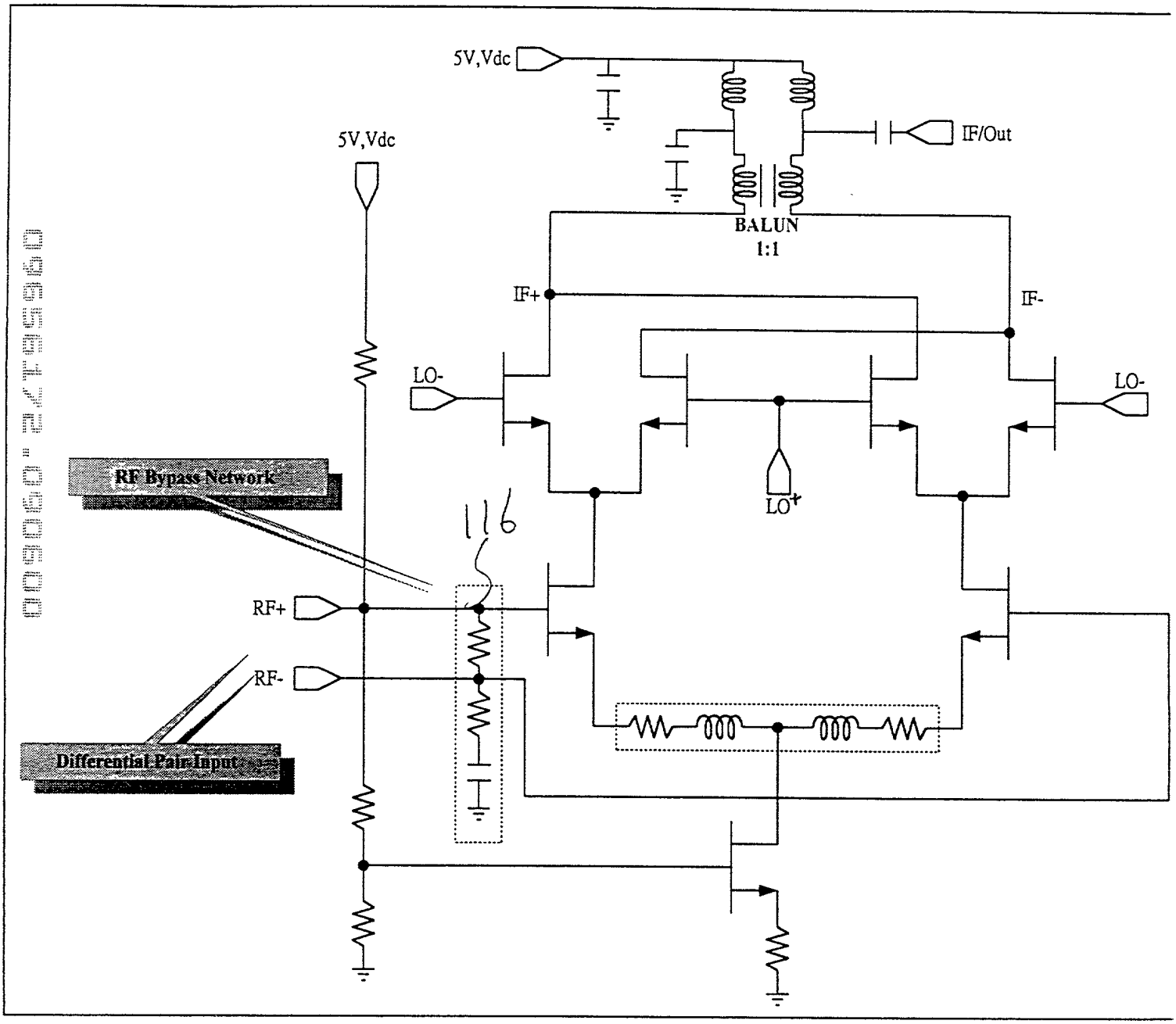


Fig. 5
PRIOR ART

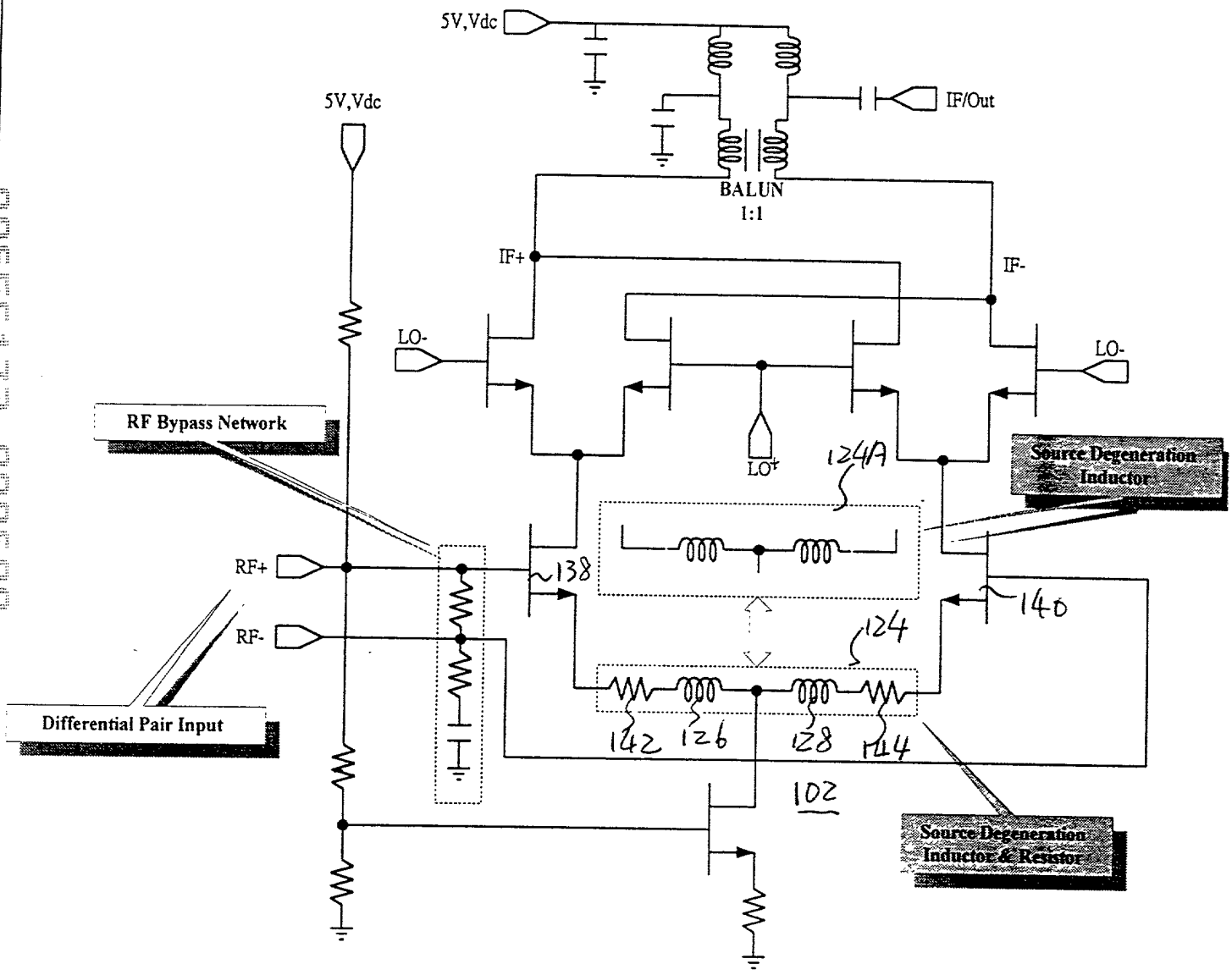


Fig. 6

PRIOR ART

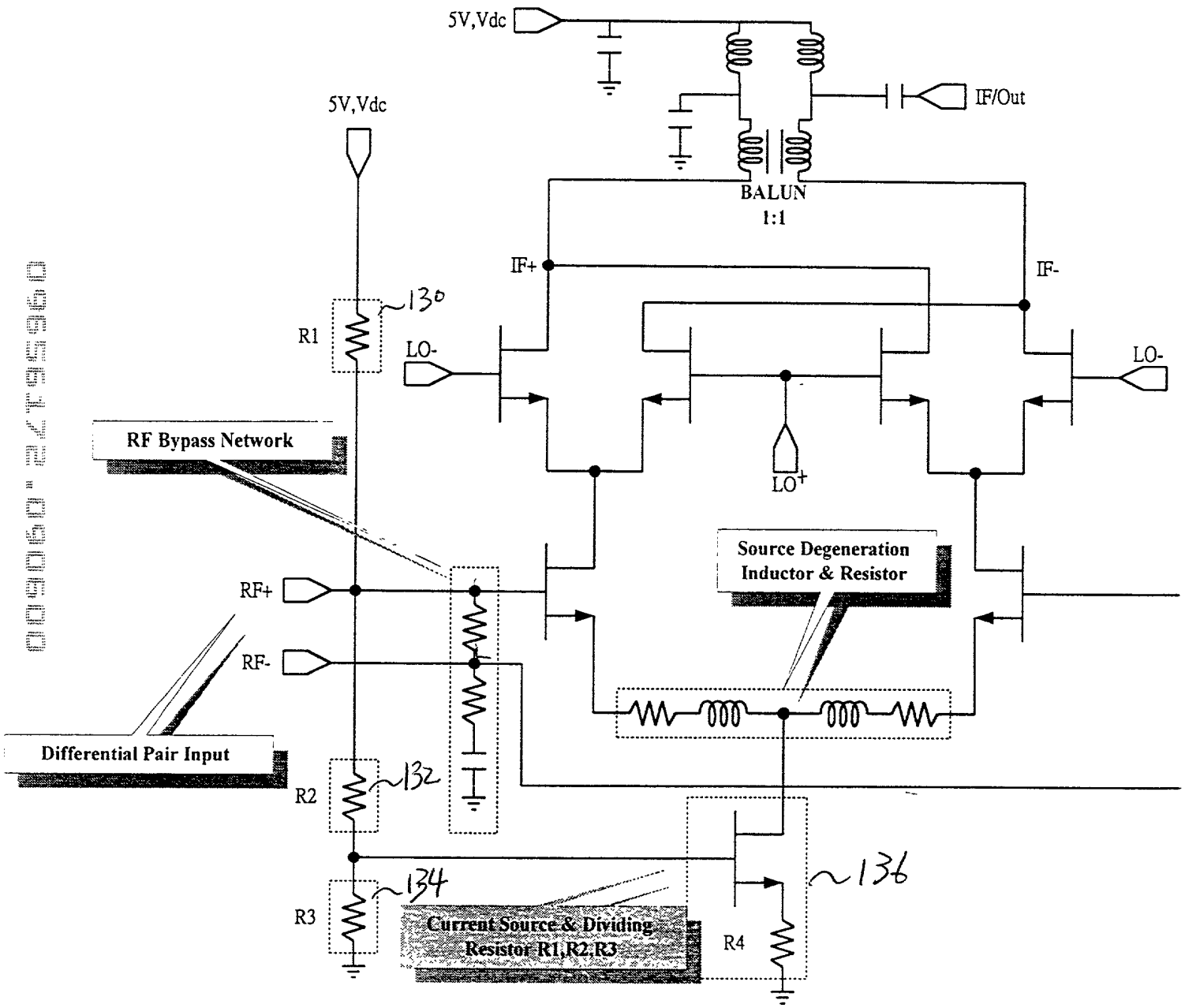


Fig. 7
PRIOR ART

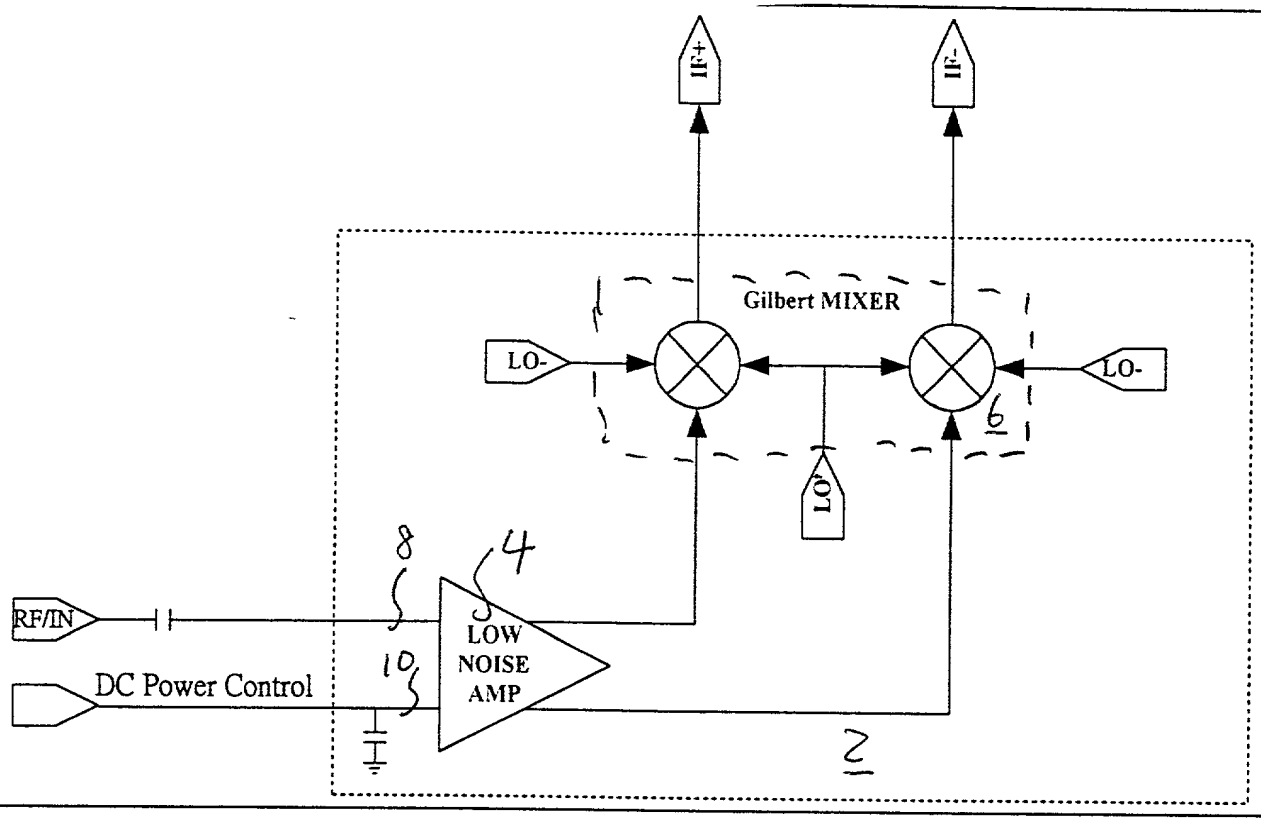

IF+
IF-
Gilbert MIXER
LO-
LO-
LO
6
8
4
RF/IN
LOW
NOISE
AMP
10
DC Power Control
2

Fig. 8

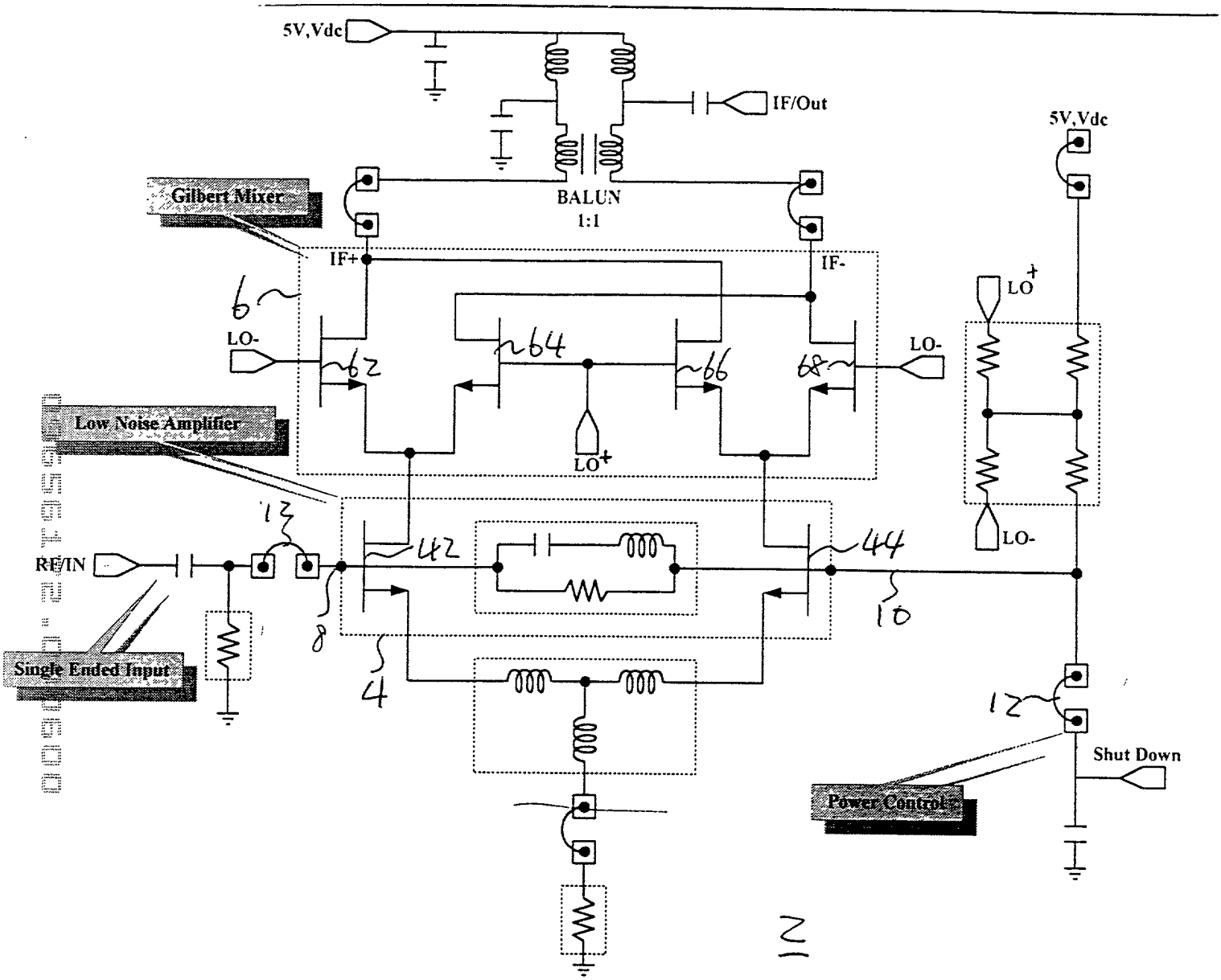

5V,Vdc
IF/Out
BALUN
1:1
Gilbert Mixer
IF+
IF-
6
LO-
62
64
66
68
LO-
LO+
Low Noise Amplifier
5V,Vdc
LO+
LO-
13
42
44
RF/IN
8
10
4
Single Ended Input
12
Shut Down
Power Control
2

Fig. 9

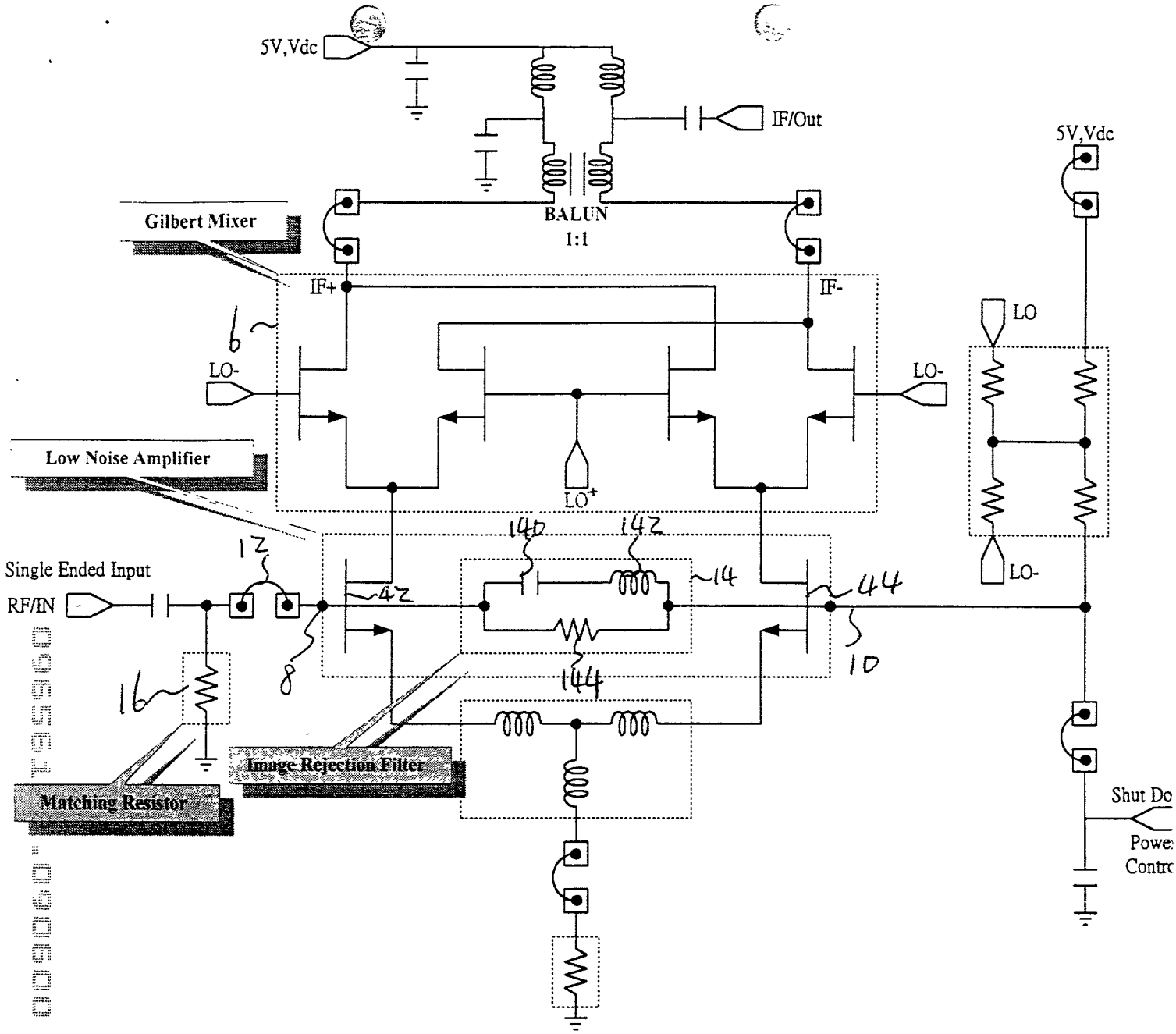

5V,Vdc
IF/Out
BALUN
1:1
Gilbert Mixer
IF+
IF-
LO-
LO-
LO+
LO
LO-
5V,Vdc
Low Noise Amplifier
Single Ended Input
RF/IN
Image Rejection Filter
Matching Resistor
Shut Do
Powe
Contr

Fig. 10

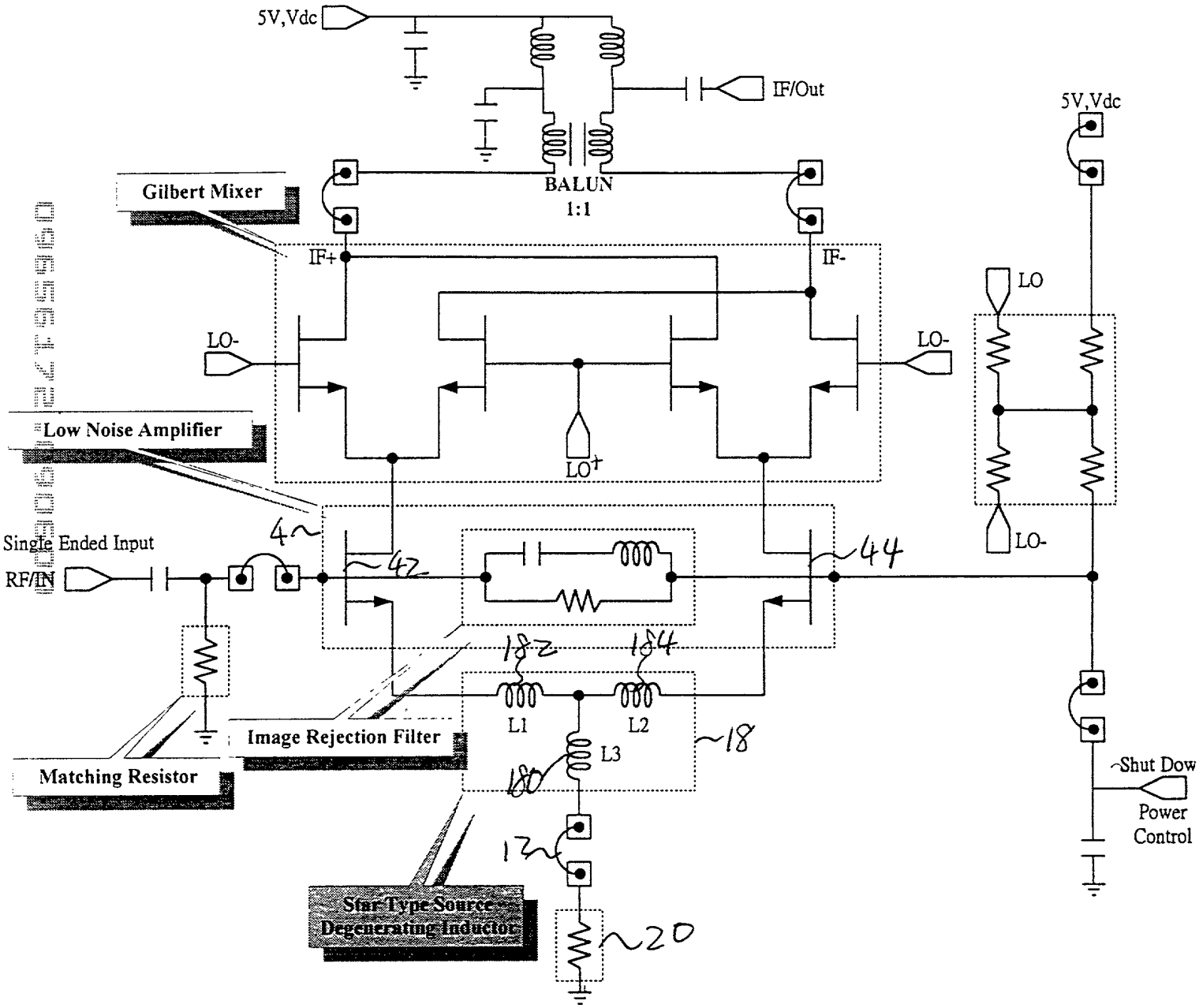

5V,Vdc
IF/Out
BALUN
1:1
Gilbert Mixer
IF+
IF-
LO-
LO-
LO+
LO
LO-
5V,Vdc
Low Noise Amplifier
Single Ended Input
RF/IN
4
42
44
182
184
L1
L2
L3
18
180
12
Image Rejection Filter
Matching Resistor
Star-Type Source
Degenerating Inductor
20
Shut Dow
Power
Control

Fig. 11

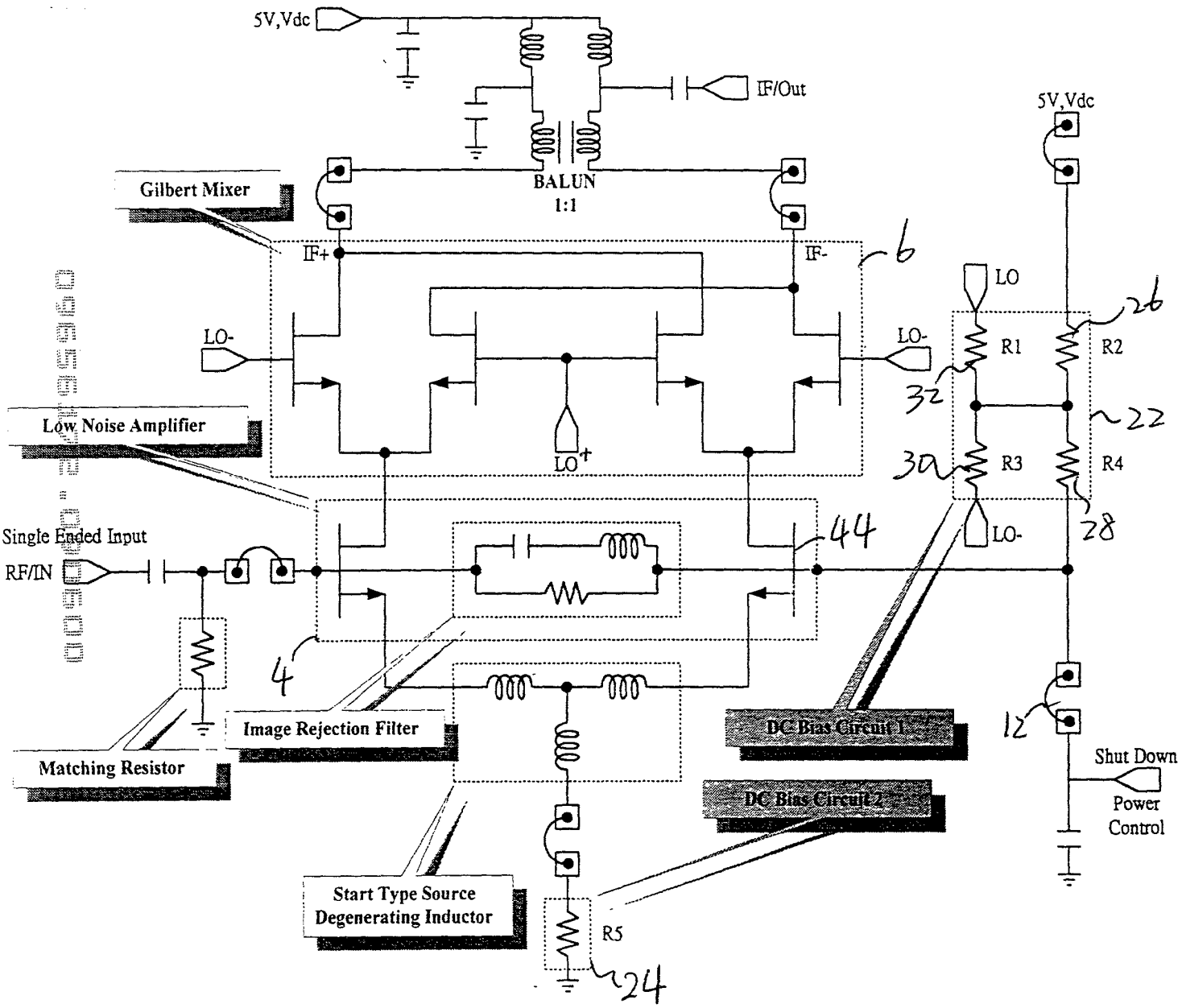

5V,Vdc
IF/Out
BALUN
1:1
Gilbert Mixer
IF+
IF-
6
LO
LO-
LO-
LO+
R1
R2
26
32
22
R3
R4
30
28
LO-
Low Noise Amplifier
Single Ended Input
RF/IN
44
4
Image Rejection Filter
Matching Resistor
DC Bias Circuit 1
DC Bias Circuit 2
12
Shut Down
Power
Control
Start Type Source
Degenerating Inductor
R5
24

Fig. 12

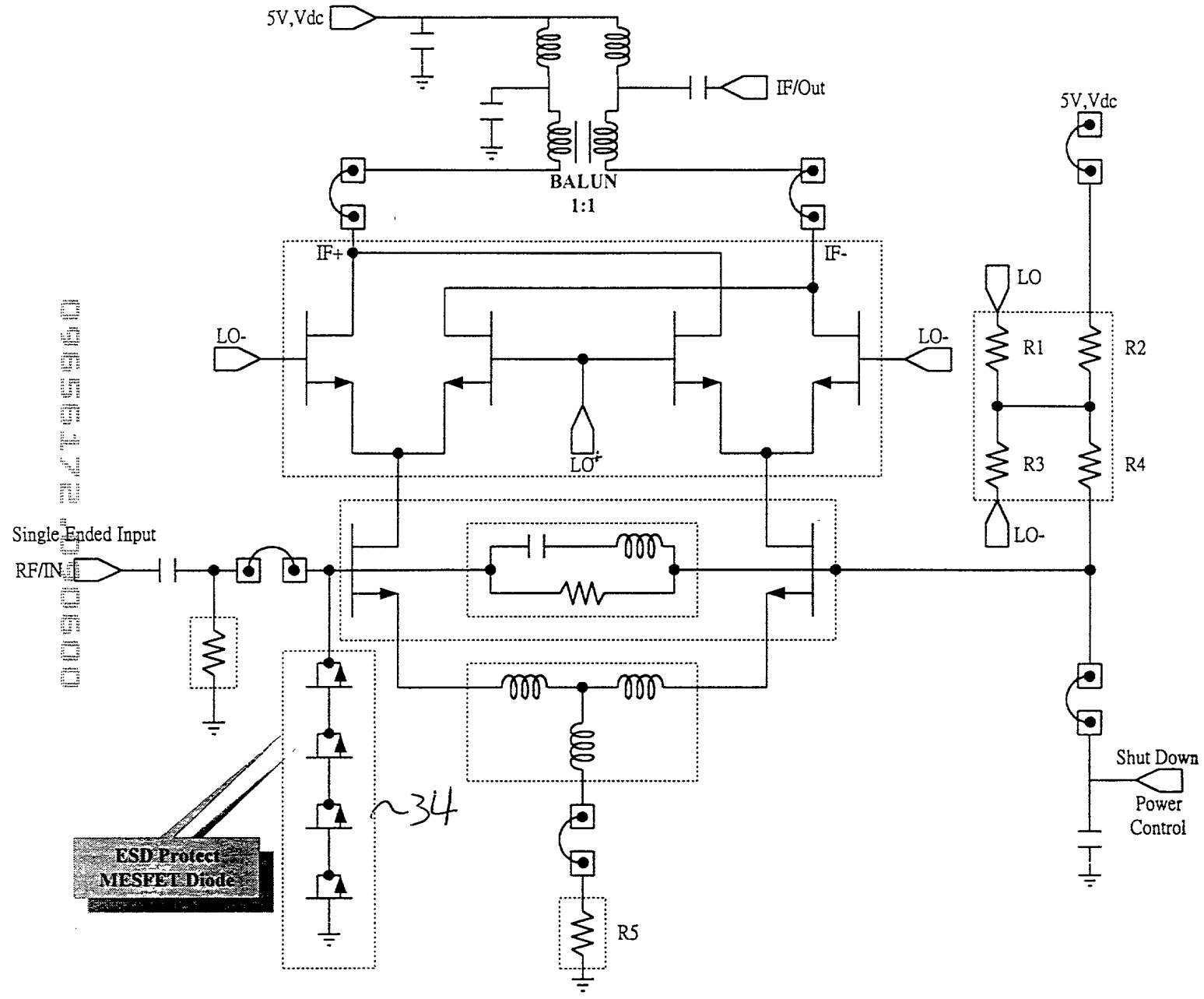

5V,Vdc
IF/Out
BALUN
1:1
IF+
IF-
LO-
LO-
LO+
5V,Vdc
LO
R1
R2
R3
R4
LO-
Single Ended Input
RF/IN
Shut Down
Power
Control
~34
ESD Protect
MESFET Diode
R5

Fig. 13

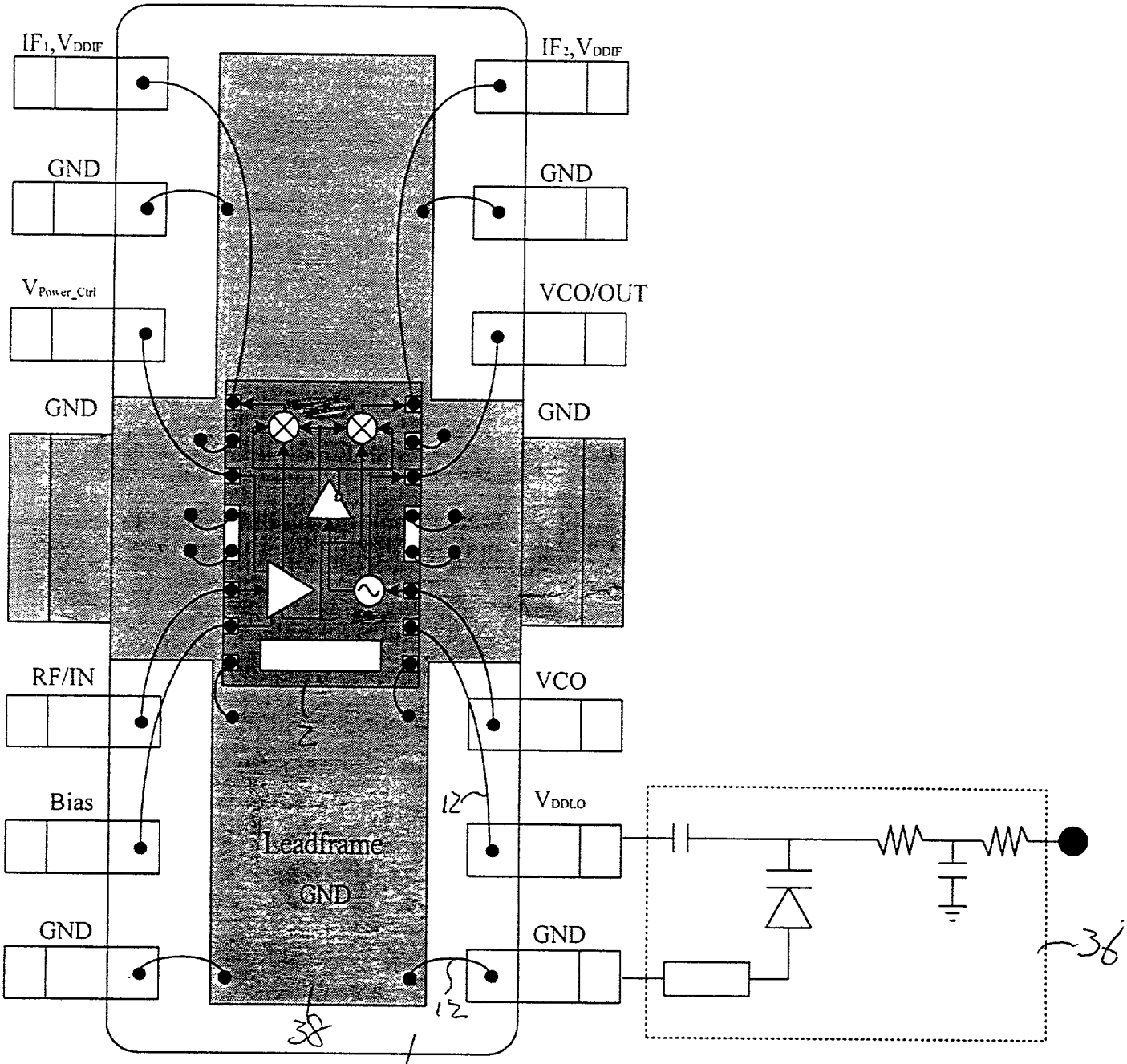

IF1, VDDIF
IF2, VDDIF
GND
GND
VPower_Ctrl
VCO/OUT
GND
GND
RF/IN
VCO
Bias
VDDLO
Leadframe
GND
GND
GND
12
12
38
40
36

Fig. 14

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, We hereby declare that: our residence, post office address and citizenship are as stated below next to our names; We believe we are the original, (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **BROADBAND SINGLE-ENDED INPUT UPCONVERTER** the specification of which is attached hereto.

We hereby state that we have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. We acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

We hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States, listed below and have also identified below, any foreign application(s) for patent or inventor's certificate, or any PCT International application(s) having a filing date before that of the application(s) of which priority is claimed:

Country	Application Number	Date of Filing	Priority Claimed Under 35
			□ YES □
			□ YES □

We hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

Application Number	Date of Filing

We hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) or § 365(c) of any PCT International application(s) designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of 35 U.S.C. § 112, We acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application(s) and the national or PCT International filing date of this application:

Application Number	Date of Filing	Status (Patented, Pending,

We hereby appoint the following attorney and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. **FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.,** Douglas B. Henderson, Reg. No. 20,291; Ford F. Farabow, Jr., Reg. No. 20,630; Arthur S. Garrett, Reg. No. 20,338; Donald R. Dunner, Reg. No. 19,073; Brian G. Brunsvold, Reg. No. 22,593; Tipton D. Jennings, IV, Reg. No. 20,645; Jerry D. Voight, Reg No. 23,020; Laurence R. Hefter, Reg. No. 20,827; Kenneth E. Payne, Reg. No. 23,098; Herbert H. Mintz, Reg. No. 26,691, C. Larry O'Rourke, Reg. No. 26,014; Albert J. Santorelli, Reg. No. 22,610; Michael C. Elmer, Reg. No. 25,857; Richard H. Smith, Reg. No. 20,609; Stephen L. Peterson, Reg. No. 26,325; John M. Romary, Reg. No. 26,331; Bruce C. Zotter, Reg. No. 27,680; Dennis P. O'Reilley, Reg. No. 27,932; Allen M. Sokal, Reg. No. 26,695; Robert D. Bajefsky, Reg. No. 25,387; Richard L. Stroup, Reg. No. 28,478; David W. Hill, Reg. No. 28,220; Thomas L. Irving, Reg. No. 28,619; Charles E. Lipsey, Reg. No. 28,165; Thomas W. Winland, Reg. No. 27,605; Basil J. Lewris, Reg. No. 28,818; Martin I. Fuchs, Reg. No. 28,508; E. Robert Yoches, Reg. No. 30,120; Barry W. Graham, Reg. No. 29,924; Susan Haberman Griffen, Reg. No. 30,907; Richard B. Racine, Reg. No. 30,415; Thomas H. Jenkins, Reg. No. 30,857; Robert E. Converse, Jr., Reg. No. 27,432; Clair X. Mullen, Jr., Reg. No. 20,348; Christopher P. Foley, Reg. No. 31,354; John C. Paul, Reg. No. 30,413; Roger D. Taylor, Reg. No. 28,992; David M. Kelly, Reg. No. 30,953; Kenneth J. Meyers, Reg. No. 25,146; Carol P. Einaudi, Reg. No. 32,220; Walter Y. Boyd, Jr., Reg. No. 31,738; Steven M. Anzalone, Reg. No. 32,095; Jean B. Fordis, Reg. No. 32,984; Barbara C. McCurdy, Reg. No. 32,120; James K. Hammond, Reg. No. 31,964; Richard V. Burgujian, Reg. No. 31,744; J. Michael Jakes, Reg. No. 32,824; Thomas W. Banks, Reg. No. 32,719; Christopher P. Isaac, Reg. No. 32,616; Bryan C. Diner, Reg. No. 32,409; M. Paul Barker, Reg. No. 32,013; Andrew Chanho Sonu, Reg. No. 33,457; David S. Forman, Reg. No. 33,694; Vincent P. Kovalick, Reg. No. 32,867; James W. Edmondson, Reg. No. 33,871; Michael R. McGurk, Reg. No. 32,045; Joann M. Neth, Reg. No. 36,363; Gerson S. Panitch, Reg. No. 33,751; Cheri M. Taylor, Reg. No. 33,216; Charles E. Van Horn, Reg. No. 40,266; and Linda A. Wadler, Reg.

No. 33,218; and Yitai Hu, Reg. No. 40,653. Please address all correspondence to **FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.** 1300 I Street, N.W., Washington, D.C. 20005, Telephone No. (202) 408-4000.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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